Designing a Scalable Topological Quantum Computer Using EUV Lithography

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Abstract

Topologically protected Majorana zero modes are expected to enable error-free quantum computing. Topology, a branch of mathematics that had little connection to condensed matter physics, deals with invariant properties of objects under continuous deformations. When applied to condensed matter systems, topology explains the robustness of certain physical properties against disorder.

Majorana zero modes are quasiparticles in 2D p-wave superconductors that are topologically protected, making them promising candidates for realizing qubits with long coherence times. In this talk, I will provide an overview of topological quantum computation and discuss how planar semiconductor processing can be used to fabricate devices that not only demonstrate the existence of Majorana zero modes but also lay the groundwork for scalable topological quantum computers. The proposed devices will be fabricated in an advanced 300mm line using extreme UV (EUV) lithography.

Although the primary focus of this talk is on topological quantum computation, the proposed device has broader applications, including quantum dot-based quantum simulators with full tunability, spin qubits without crowding issues, and on-demand quantum emitters.

Biography: Prof. Ji Ung Lee

Prof. Lee received his PhD in Electrical Engineering from the University of Wisconsin-Madison (1996). He joined CNSE in 2007. His interest is in designing and characterizing nanoscale devices. His current interest is in fabricating a scalable topological quantum computing chip using 300mm fabrication line, with the emphasis on using EUV lithography.